A10

reference clock while said n is a positive integer, and whereby a frequency of the output clock is $1/(tCK-\Delta\Phi)$.

IN THE DRAWINGS:

Please amend FIG. 27 of the drawings as shown in red in the attached copy of the drawing.

REMARKS

The specification has been amended to correct minor clerical errors.

FIG. 27 has been amended per the Examiner's request. Corrected formal drawings will be filed upon allowance of the Application.

Claims 1 and 28 have been amended to clarify the invention. The allowability of claims 33-35 has been noted with thanks. Claim 33 has been rewritten in independent form, and claims 34 and 35 have been amended to correct minor typographical errors. No new matter has been entered.

Pursuant to 37 CFR § 1.121, marked copies of the amended specification paragraphs, claims and drawings showing changes made therein accompany this Amendment.

Turning now to the rejection of claims 1, 28, and 31 as anticipated by Shieh et al., U.S. Patent No. 6,323,705, claims 1 and 28 have been amended to require that the unit of addition or subtraction from the phase of the reference clock be determined for each clock "cycle" of the reference clock. This clearly is not taught or suggested by Shieh et al., where the phase shift of the output clock relative to the input clock is controlled by a shift register set by a feedback loop (see Figure 2). Because Shieh et al. teaches a feedback loop to set the phase shift unit for the clock output, the phase of the output clock is not optimum until the second clock cycle. Since claims 1 and 28 require that each cycle of the reference clock produce an output clock whose

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phase is shifted by a predetermined amount, claims 1 and 28 are not taught by Shieh et al. Thus, claims 1 and 28 and all claims dependent thereon cannot be said to be anticipated by Shieh et al.

Turning to the rejection of claim 29 as obvious from Shieh et al. in view of Tanis et al., U.S. Patent No. 5,258,724, claim 29 is dependent on claim 28. The deficiencies of the primary reference Shieh et al. vis-à-vis claim 28 are discussed above. It is not seen that Tanis et al. supplies the missing teachings to Shieh et al. to achieve or render obvious claim 28 or claim 29 which depends thereon. Tanis et al. has been cited as teaching a fractional division synthesizer comprising a fractional divider, and is acknowledged as so teaching. However, the more basic and essential claimed features missing from Shieh et al. are not found in Tanis et al. Thus, no combination of Shieh et al. and Tanis et al. reasonably could be said to achieve or render obvious claim 28 or claim 29 which depends thereon.

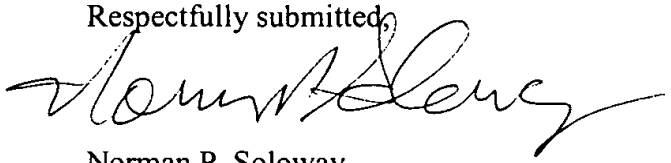
Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance.

If the Examiner desires personal contact for further disposition of this case, the Examiner is invited to contact the undersigned attorney at (520) 882-7623.

Form PTO-2038 authorizing a credit card payment in the amount of $84.00 for the added independent claim fee is attached.

In the event there are any fee deficiencies or additional fees payable, please charge them (or credit any overpayments) to our Deposit Account No. 08-1391.

Respectfully submitted,



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MARKED COPY OF SPECIFICATION PARAGRAPHS

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MARKED SPECIFICATION PARAGRAPHS SHOWING CHANGES MADE

Paragraph bridging pages 1 and 2, beginning at page 1, line 22:

For example, there is proposed in JP Patent Kokai JP-A-11-284497 a programmable delay generator in which a ramp waveform voltage for determining a delay time and a threshold voltage can be generated by circuits of the same structure and can be independently set so that it is capable of generating the delay time of a fractional number, a numerator and a denominator of which can be set, a frequency synthesizer which, by phase-interpolating output pulses of an accumulator using [the] a programmable delay generator, is able to generate an adjustment-free low-spurious output signal, a multiplication circuit employing [the] a programmable delay generator, a duty ratio converter circuit employing the programmable delay generator as an output pulse width setting delay generator, and a PLL frequency synthesizer having the programmable delay generator inserted between the frequency divider and a phase comparator.

Paragraph beginning at page 3, line 3:

For accomplishing the above object, [in accordance with] one aspect of the present invention is [provided] a configuration in which a clock is input and an output clock having a phase difference relative to the input clock, the phase obtained by adding or subtracting to or from said phase by a predetermined unit value of a phase differential, on each constant period, is output.

Paragraph beginning at page 3, line 10:

In accordance with another aspect of the present invention, a clock control circuit comprises control means for outputting a control signal for adding or subtracting to or from [a] the phase of an output signal relative to a reference clock, which is an input clock or a clock

generated from the input clock, on each clock period of the reference clock, and phase adjustment means fed with the input clock for generating and outputting output clock having a phase corresponding to [addition or subtraction] adding or subtracting a preset unit value of a phase differential to or [form] from a phase with respect to the reference clock, based on the control signal, whereby an output clock of a frequency in a non-integer relation [with respect] to [th] the frequency of the reference clocks can be output.

Paragraph bridging pages 3 and 4, beginning at page 3, line 22:

[In accordance with a]Another aspect of the present invention[,] is [also provided] a clock control circuit comprising a frequency divider for outputting frequency-divided clock obtained on frequency dividing the input clock, a control circuit for generating a control signal for adding or subtracting a unit phase difference to or from the input clock with respect to the frequency-divided clock based on the frequency divided clock output from the frequency divider and a phase adjustment circuit fed with the input clock and generating and outputting an output clock having a phase prescribed by the control signal from the control circuit.

Paragraph beginning at page 4, line 7:

[In accordance with a]Another aspect of the present invention[,] is [provided] a clock control circuit comprising a multi-phase clock generating circuit for generating and outputting first to nth clocks having respective [difference] different phases(multi-phase clocks) from a phase of the input clock, a selector fed with the first to nth clocks to selectively output one of the clocks, and a control circuit fed with the input clock to generate a control signal sequentially selecting the first to nth clocks to send the generated selection signal to the selector.

Paragraph beginning at page 4, line 15:

[In accordance with a]Another aspect of the present invention[,] is [provided] a clock control circuit comprising an interpolator receiving a frequency divided signal produced by a frequency dividing circuit receiving a clock signal and a signal obtained by shifting the frequency divided signal in a preset number of periods of the clock to produce a signal obtained on division of a timing difference of said two input signals at a preset ratio of internal division; and

a control circuit for varying the value of the ratio of the internal division of the timing difference in said interpolator based on said clock signals.

Paragraph bridging pages 4 and 5, beginning at page 4, line 25:

[In accordance with a]Another aspect of the present invention[,] is [provided] a clock control circuit comprising a plurality of (N) interpolators for outputting signals obtained on dividing a timing difference of two input signals with respective different values of a preset ratio of internal division; wherein of first to nth clocks with respective different phases, two clocks, that is the Ith and the (I+1)st clocks, where I is an integer from 1 to N, with N+1 being 1, are input to the Ith interpolator.

Heading at page 10, line 17:

[PREFRRED] PREFERRED EMBODIMENTS OF THE INVENTION

Paragraph bridging pages 10 and 11, beginning at page 10, line 18:

Preferred embodiments of the present invention are described [in the bellow] below. In a preferred embodiment of the present invention, a clock control circuit comprises a control circuit (102 of Fig.1) for outputting a selection control signal for selecting incrementing (adding) or decrementing (subtracting) to or from a phase relative to a reference clock[,] by a predetermined unit value of a phase differential on each reference clock cycle, which is an input clock or a

clock generated from an input clock; and a phase adjustment circuit (101 of Fig.1) fed with the input clock and generating an output clock having a phase corresponding to incrementing or decrementing a predetermined unit phase value of a phase differential with respect to the reference clock, based on the control signal, whereby an output clock of a frequency in a non-integer relation with respect to the frequency of the reference clock can be output.

Paragraph beginning at page 11, line 7:

In another preferred embodiment of the present invention, a clock comprises a frequency divider (103 of Fig.3) for outputting frequency-divided clocks obtained by frequency dividing the input clock, a control circuit (102 of Fig.3) for generating a control signal for adding or subtracting to or from a phase by a unit phase differential relative to the input clock with respect to the frequency-divided clocks based on the frequency divided clocks' output from the frequency divider, and a phase adjustment circuit (101 of Fig.3) fed with the input clock and generating and outputting an output clock having a phase prescribed by the control signal from the control circuit.

MARKED COPY OF AMENDED CLAIMS

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MARKED CLAIMS SHOWING CHANGES MADE

1. (Amended) A clock control circuit comprising:

[means] a circuit for generating and outputting an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a predetermined unit value of a phase differential on each clock [period] cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock.

28. (Amended) A clock control method comprising the steps of:

generating an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a [predetermined] unit value of a phase differential on each clock [period] cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock; and

outputting said output clock.

33. (Amended) [The] A clock control method [as defined in claim 28] comprising the steps of:

generating an output clock having a phase relative to a reference clock by adding or subtracting to or from said phase by a unit value of a phase differential on each clock cycle of said reference clock, said reference clock being an input clock or a clock derived from the input clock; and

outputting said output clock wherein the output clock is phase-adjusted by an interpolator outputting a signal, a propagation delay of said signal corresponding to division of timing difference of two clock signals to vary ration of internal division of timing difference of said

interpolator to enable outputting of an output clock of a frequency which is [an] a non-integer frequency of the input clock frequency.

34. (Amended) A clock control circuit comprising:

a circuit that receives an input clock and generates an output clock with a phase relative to a reference clock being changed on each cycle of the output clock, said reference clock being the input clock or a clock derived from the input clock, wherein a phase of the output clock relative to the reference clock for another cycle next to one cycle is produced by adding to the phase of the output clock corresponding to said one cycle a unit phase differential value $\Delta\Phi$, where the $\Delta\Phi$ is a predetermined value such that $n\Delta\Phi$ is equal to one clock period(tCK) of said reference clock while said n is a[n] positive integer, and whereby a frequency of the output clock is $1/(tCK+\Delta\Phi)$.

35. (Amended) A clock control circuit comprising:

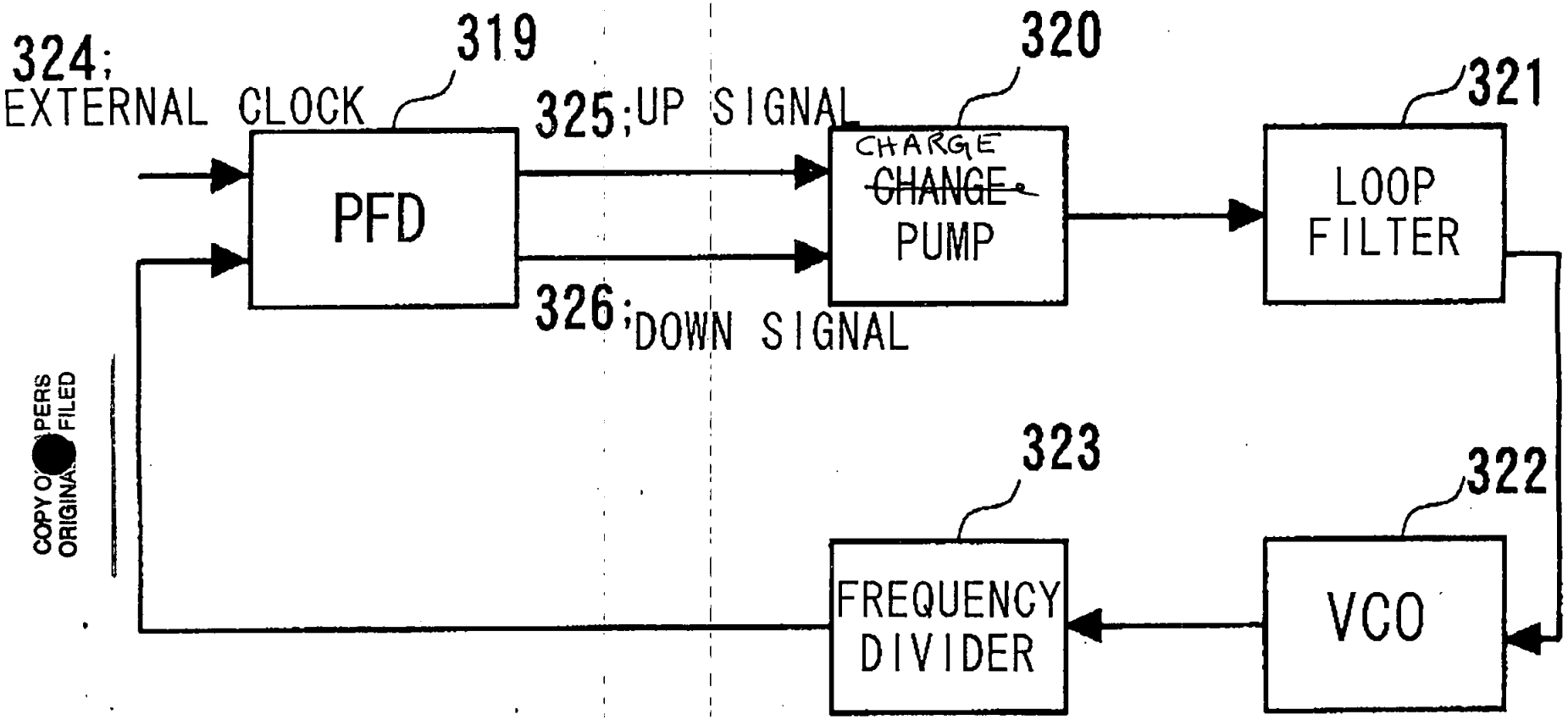
a circuit that receives an input clock and generates an output clock with a phase relative to a reference clock being changed on each cycle of the output clock, said reference clock being the input clock or a clock derived from the input clock, wherein a phase of the output clock relative to the reference clock for another cycle next to one cycle is produced by subtracting from the phase of the output clock corresponding to said one cycle a unit phase differential value $\Delta\Phi$, where the $\Delta\Phi$ is a predetermined value such that $n\Delta\Phi$ is equal to one clock period(tCK) of said reference clock while said n is a[n] positive integer, and whereby a frequency of the output clock is $1/(tCK-\Delta\Phi)$.

MARKED DRAWINGS

SERIAL NO. 09/910,117

DOCKET: NEC G226

FIG . 27 PRIOR ART



Approved by Examiner [illegible] 10/29/02